Grounding and Shielding Issues

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Grounding issues:

- Where/how are different grounds connected

Shielding issues:

- How are cables shielded, the need for a commoning shield integrated with the pixel Global Support, and what is the shielding role of the beampipe.

Grounding and Shielding Concept:

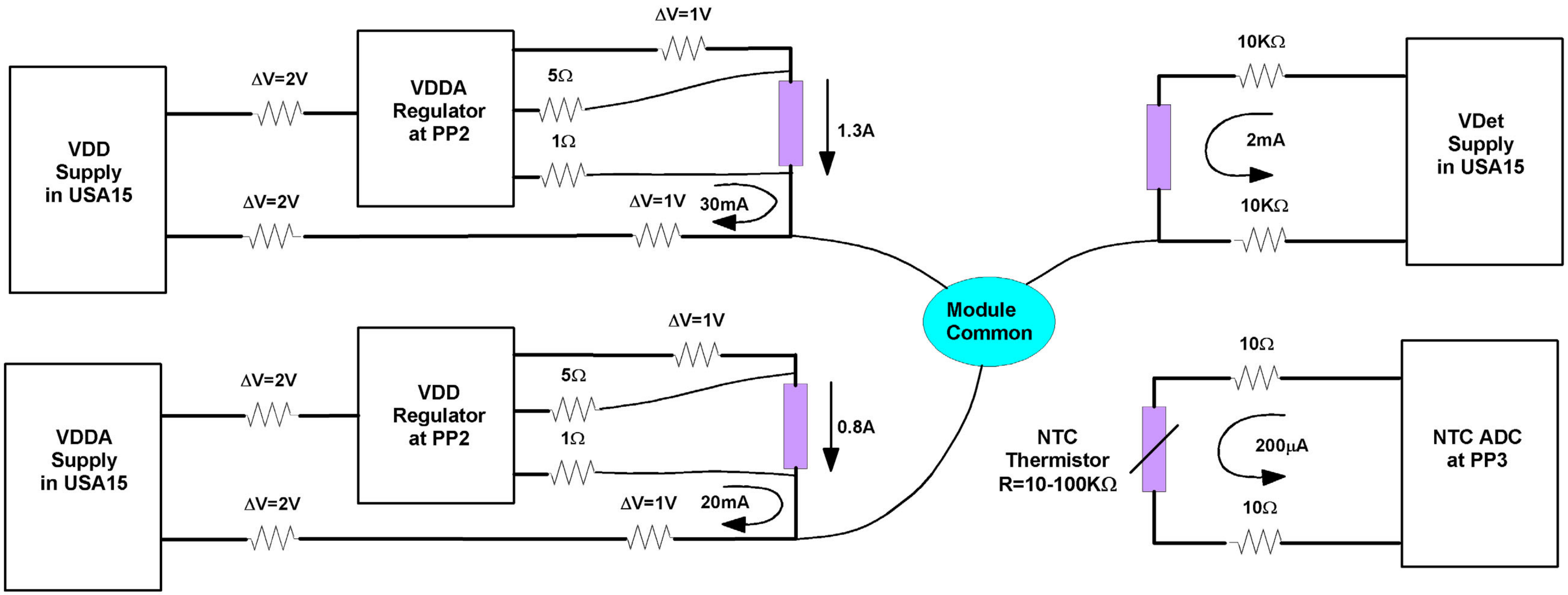
Grounding Philosophy:

- All power supplies are assumed to have individually floating channels within each complex channel. Only safety (high impedance) ground connections are made at the supply end. All low-impedance grounding/commoning takes place inside the detector volume. The connection between the pixel detector commoning point (see below) and the rest of ATLAS should be through a controlled, single-point connection, not the result of many random connections.
- Initial reference point will be connection of various grounds on module. The present grounds are AGnd (VDDA return and VDET return) and DGnd. Interconnections of these grounds can be individually controlled on Flex Hybrid. However, note that this hybrid does not have a ground plane, but only rather narrow ground traces, which only barely satisfy our ΔV requirements due to limited area available in first-generation double-sided designs.
- Second reference point would be connection of relevant grounds at PP0 patch panel. Imagine that would connect AGnds from all modules in a service bundle, and connect DGnds from all modules in a service bundle. There could be the option of connecting AGnd and DGnd also at this level, but this is not preferred.
- Final reference would be the overall Commoning Point for the detector. In the original insertable design, in which B-layer replacement in situ was required, this point was at PP1. It might be possible to move this point to PP0.

- Overall concept is similar to SCT, and has a shield at the outer radius (on the Pixel Support Tube) which serves as the commoning point for all local grounds, and which would shunt the externally induced noise currents on these grounds around the sensitive signal paths inside the individual modules.
- This Aluminum cylinder would be created on the outer wall of the Support Tube in the new pixel mechanical design, and is essential. Detailed calculations are needed for its thickness, but something like 50-100μ of Al seems reasonable. It should be thick enough that there is a significant reduction in the noise current flow through the module signal paths (at least factor of 10). This implies that the relative impedance of the shunted current paths should be at least ten times lower than the impedance for noise currents to flow through the signal paths.
- For the original concept, in which the B-layer installation was required to be possible in situ, the only practical possibility for such a commoning point was PP1. PP0 was not practical because it is almost impossible to implement a real shield (continuous metal layer) in this region due to mechanical constraints, so only a shunt could be provided. Connection to beampipe at PP0 was also hard.
- With the new "package" concept, where integration with the beampipe and B-layer is performed on the surface, a more integrated scheme is possible. It should be possible to implement the Faraday Cage and Commoning Point at PP0 instead of PP1. In this case, the pixel detector would be shielded around the Global Support Structure instead of around the Pixel Support Tube. This greater flexibility will be explored in more detail in the near future.

- Expect that service bundles (half-stave or sector level) from PP1 out are individually shielded with overall foil wrap of 50μ of Al, or enclosed in individual conductive (but isolated) Al cable trays. These shields should be connected together at commoning point, and should surround cables from PP1 outwards. Individual foil shields should not be in electrical contact as cables find their way out from commoning point, to avoid additional ground loops between the shields.
- The pigtails, as well as the cables going inside from PP1 to PP0, should not require shielding from the point where they enter the Support Tube Shield until they connect to the individual modules, but this depends somewhat on whether a good low-EMI design is possible for the cables. One concern is that with the present opto-card location, the Type 0 cables to PP0 contain the fast clock and data lines (albeit as LVDS pairs). It may be necessary to shield each cable from the noise produced by the other cables.
- The pixel volume would be further enclosed by the conductive sheet at the end of the support tube, that would be used to connect the beampipe and the Aluminum support tube shield together electrically. PP1 itself makes this very challenging.
- The above scheme works best if the central portion of the outer wall of the beampipe is electrically isolated from the inner wall of the beampipe. This appears too difficult, so we will try to implement an additional thin foil shield between the B-layer and the beampipe to complete the Faraday cage for pixels. Would then connect the Support Tube Shield to one end of the beampipe to avoid creating loops for the beam image currents to flow around.

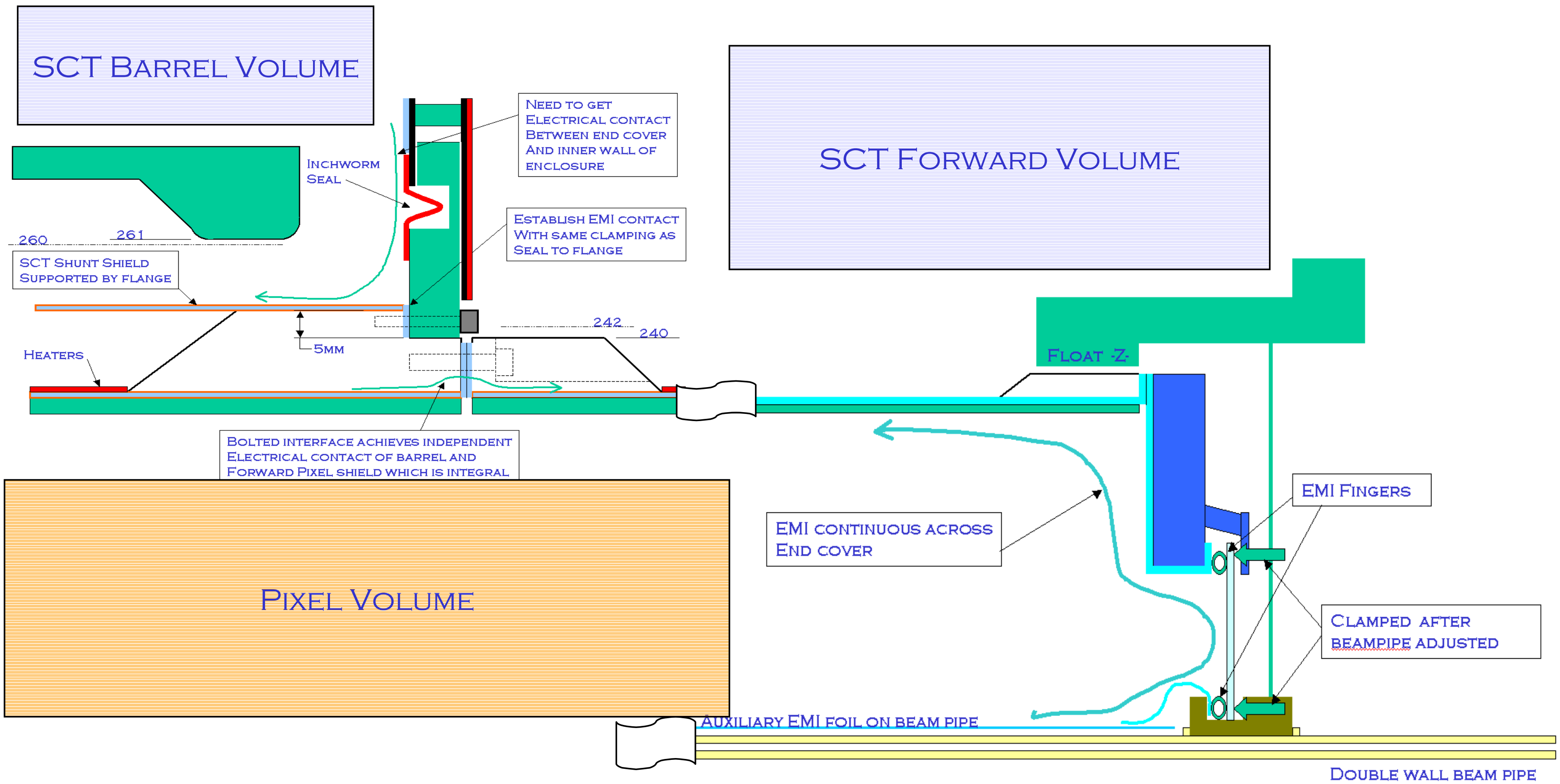
Concept for power supply connections to module:



- Ideal situation is to have the Module Common point as the only commoning point for the current flows in the regulator error amplifiers. The NTC ADC (operating in voltage excitation mode with a 2V supply) would be isolated. Both sides of the HV supply are isolated by series resistors (may need to common return line).
- For the present L4913, there is significant current flowing in the sense return line (about 2% of load current) used to control pass transistor. This requires large lines for sense return, and also reduces the load regulation, as sensed voltage will depend on load current.
- Separate sense return lines for analog and digital supplies are used to minimize analog/digital coupling in system.

Summary of the Overall Grounding/Shielding Scheme

- Form Faraday cage from 7m long Support Tube and outer beampipe wall:

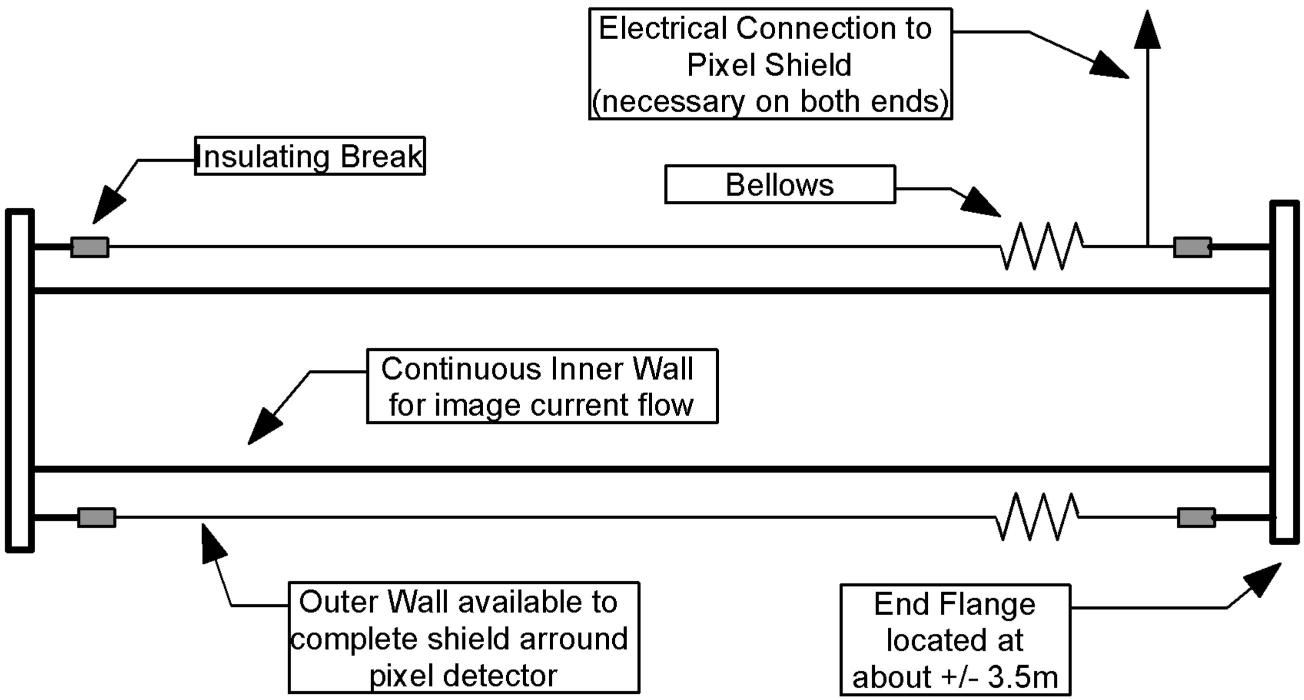


- Outer wall of Support Tube is metalized and connected to metalized Endplugs.
- Electrical connection is made to the beampipe as well, with the possibility of an additional very thin shielding layer to close Faraday cage.
- All cables from PP1 outwards are shielded in their trays in a “star” topology.

Beampipe Issues

Present baseline is double-wall beampipe:

- This design offers many advantages from grounding/shielding point of view. The dangerous beam image currents flow on the inner wall, and the outer wall could be available to play a significant role in defining a shielding cage for pixels.
- Beampipe concept, with both inner and outer walls of 800μ thick Be:

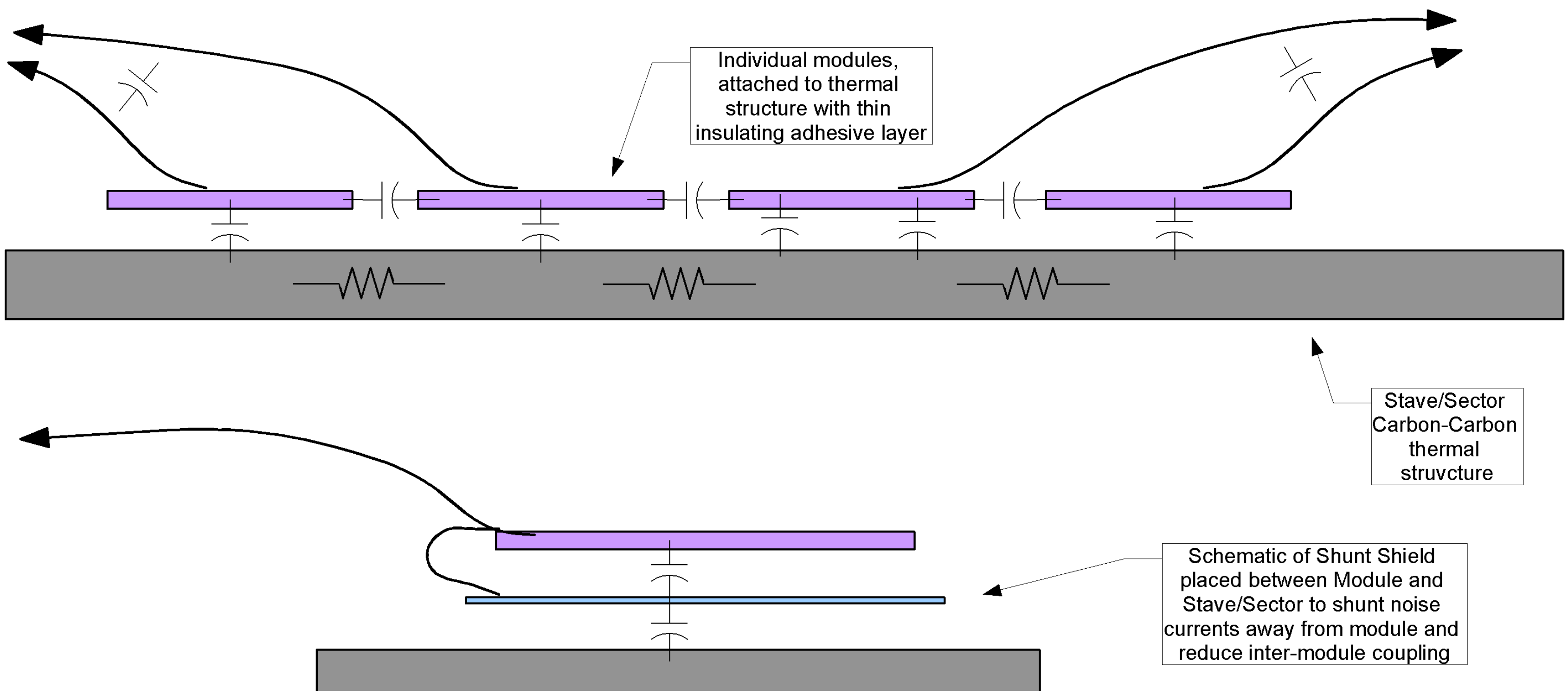


- Recent comments from beampipe experts suggest that electrical isolation of central portion of outer beampipe by insulating breaks is technically too difficult and risky to implement in first version.

Module attachment issues/comments:

- Local mechanical supports are all electrically conductive C-C material (few ohms). The modules are assumed to be electrically (DC) isolated from these structures, but they are mechanically intimately coupled to them. The exact scheme depends on whether or not back-side AGnd connection to the module is needed. If it is not needed, then the chip back-side is coupled via about 100μ of adhesive (ε=4, 100μ thick gives 35pF/cm^2, or 500pF/module). This will connect all module grounds together via a moderate impedance in the frequency range of greatest relevance (impedance of ideal capacitor of 500pF is 100Ω at 3.5MHz).

Electrical Model of Module Coupling in Stave/Sector



- Shunt Shield between module and thermal structure offers the possibility of increased isolation between modules on common thermal structures. However, it certainly complicates the module attachment and degrades the thermal conductivity between module and cooling pipe.

Comments on back-side electrical contact with module:

- The substrate of an FE chip is made out of low-resistivity (highly doped) p+ material. In the case of the DMILL SOI process, there is a 1.2μ epitaxially grown layer of silicon which is on top of a buried oxide layer, and so the silicon in which the transistor wells are formed is only capacitively coupled to the wafer substrate. In the case of a deep-submicron process, there is a 2μ epitaxially grown layer on top of a very highly doped p+ substrate (resistivity < 0.01Ω-cm), and there is a direct coupling to the wafer substrate.
- In either case, any digital noise currents flowing in the substrate could change the potential of the wells of analog transistors, and therefore have the potential to affect the noise performance of the FE chip. If the back of the low-resistivity substrate is instead uniformly connected to a high quality ground plane, then these noise currents will tend to follow the path of lowest impedance down through the substrate to the ground, and not couple into nearby sensitive analog circuits. Conservative practice would always connect the back-side to ground.

- This has been tested in earlier generations of FE IC's (FE-B and FE-D1b) by back-side grinding (to remove native oxides), and plating with Ni and Au. The die were then epoxied to the standard single-chip support card, which contains a large analog ground plane under the entire FE die region. In none of these cases did we detect a significant change in noise performance for the two cases (with and without low-impedance back-side contact). For the FE-B case, this was tested on bump-bonded assemblies from both IZM and AMS, both single chips and modules. For the FE-D1b case, this was only tested with bare die.
- Nevertheless, particularly with the FE-I design, it is possible that once we arrive at final FE designs, there will be a large difference between the noise performance with and without the good back-side contact.
- It is very difficult to implement an elegant back-side contact scheme for ATLAS pixel modules. A major issue with any ground plane is that a large metal plate has a much larger CTE than the carbon structure. This means that the large metal pad for contacting the back-side must be divided into small regions. Furthermore, the present 2-sided Flex design does not contain a true ground plane, increasing the interest in having the support interface fill this need.
- These issues will be explored in detail over the coming year using 0.25μ modules on stave and sector prototypes. If it is necessary, we will revisit possible mechanisms for making backside module ground connections.

Additional issues/comments:

- It is assumed that the local mechanical supports will in general be electrically (DC) isolated from the relevant support shells (barrel) and support rings (disks). There should be a decent quality single-point ground connection between all elements of the mechanical support structure, to provide a safety ground and keep the mechanical structure at a well-defined potential without ground loops. This does not have to be a low-impedance connection. This safety ground should be single-point connected to global common forming a “ground tree”.
- For the barrel case, would prefer the connection to be on one end only to prevent individual staves shunting the outer shield. It seems to be impossible to electrically isolate the two halves of a stave via the joint used in the stave fabrication. The capacitive coupling of modules to the common stave then provides the lowest impedance parasitic current path. For disk case, all individual sectors are isolated from each other, and from the overall mechanical support, by a small PEEK insert.
- Present cooling concept involves a bi-stave (both cooling connections at the same end of a pair of staves) and a double sector for new 8-sector disks. The bistave case has the pair of pipes close together (few cm), but the disk case has the pipes about 90 degrees apart in ϕ. This makes commoning of the relevant stave pipes topologically simple, but for the disk, only one end should be commoned.

- Insulating break in both inlet and exhaust cooling pipes at PP1 is highly desirable, although the implementation for the larger diameter exhaust pipe is more difficult. The isolated portion of the cooling pipes inside PP1 would be connected to the commoning point vua a “safety ground” as described previously.
- Finally, most of the conductors in the above discussion are Aluminum, and there are many issues involved in making reliable, low-resistance connections between and to these conductors (the connection resistance must remain low over a multi-year lifetime).

Summary

- Need to perform electrical characterization of carbon-carbon in Stave/Sector prototypes and carry out detailed electrical modeling of fully populated structures.
- Need to make sure that evolving beampipe design provides best Faraday cage possible within other constraints, and includes proper electrical contact points. Will consider introduction of additional screening layer to close Faraday cage since it appears impossible to isolate outer wall of beampipe.
- Need to re-examine shielding scheme with PP1 Commoning Point, and see if this can be moved in to PP0 Commoning Point.
- Need to include appropriate metalization of new Support Tube in design to be sure we provide a low-impedance shielding and shunting path for noise currents.
- Need to begin multi-module system tests as soon as possible to investigate whether shunt-shields between modules and support structure are needed. Also need to further explore how module attachment would be modified if a shunt shield is needed, a back-side chip connection is needed, or both are needed.
- Need to prototype different grounding schemes for pigtails and PP0, with full length power cables. Of particular concern is the case of barrel modules whose services run out in opposite directions from the detector, where the loop area of the services bundles is very large.